Analysis and Elimination of Parametric Oscillations in Monolithic Power Amplifiers

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Abstract — **This work describes an analysis and design methodology for eliminating parametric oscillations in microwave power amplifiers. Large-signal stability analyses based on system pole-zero identification techniques are proposed to guide the design process towards a stable circuit. In order to demonstrate the proposed approach, parametric oscillations of a Ku-band MMIC power amplifier have been eliminated, while maintaining the original performances of the circuit.**

I. Introduction

Success in design of monolithic power amplifiers relies on several critical points, such as the choice of an adequate technology, the availability of reliable non-linear models of the transistors, the utilization of powerful CAD tools and the application of appropriate analysis and design approaches. The multistage topology of most power amplifiers makes them very prone to the presence of parametric oscillations (spurious signals of autonomous nature that show up as a function of input power or input frequency) due to the presence of multiple non-linear elements and feedback loops [1], [2]. It is necessary to adopt correct analysis strategies at the design stage to detect and avoid the presence of these undesired responses, especially in the case of monolithic technologies since circuit modification is not possible after fabrication. In particular, when working with harmonic balance simulators, a two-step procedure is required. First, large-signal stability analyses need to be included in the design cycle in order to detect the possible start-up of any parametric oscillation. Second, suitable information must be extracted from the stability results so that the designer can judiciously modify the circuit in order to eliminate any risk of oscillation.

In this work a specific analysis strategy is proposed to avoid parametric oscillations in power amplifiers. It is based on a large-signal stability technique that determines the system poles and zeroes associated to the linearization of the simulated large-signal response of the power amplifier [3]. Apart from giving graphical and accurate information about the possible spurious oscillations, the technique provides the relative degree of stability of the large-signal response under analysis. Based on this knowledge, specific design approaches are incorporated to ensure the stability of the amplifier.

The proposed approach has been used here to analyze the parametric oscillations of a Ku band MMIC power amplifier, whose first version turned out to be unstable, and to eliminate these oscillations in a second version of the circuit.

II. Large-Signal Stability Analysis of Multistage Power Amplifiers

The technique proposed in [3] is adapted here to the large-signal stability analysis of multistage amplifiers simulated with Harmonic Balance (HB). This technique is based on the calculation of the system poles and zeroes associated to the linearization of the simulated large-signal steady state. This linearization is performed by injecting a small-signal current perturbation i_n, at a given frequency, into a node n of the circuit and observing the voltage response v_n at this node at that given frequency. A frequency sweep of the perturbation current generator allows to obtain the closed-loop frequency response defined as $H_{cl}^n(j\omega) = v_n / i_n$. Then, the application of system identification methods to this frequency response provides the circuit poles. The stability of this steady-state solution is guaranteed if no poles with positive real part are obtained.

In theory, except for exact pole-zero cancellations all the possible $H_{cl}^n(j\omega)$ associated to the different nodes in the circuit share the same characteristic equation [4]. Therefore, any of them contains the required information about the circuit stability of the analyzed steady state. In practice, however, when analyzing multi-stage microwave

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amplifiers, numerical problems related to the filtering effect of the matching networks can arise in the determination of the system poles. A particular instability generated in one stage may or may not be detected if the probe is connected at a different stage. Therefore, one analysis per stage is required to obtain the complete stability information.

Once unstable poles have been detected at a stage, their position in the pole-zero map provides a graphical information about their relative stability margin. Moreover, the evolution of these critical poles in the map versus any circuit parameter supplies invaluable information to help stabilize the amplifier.

In order to extract all this stability information while designing the amplifier, multiple stability analyses are required. Therefore, the stability technique needs to be agile and low time-consuming. The proposed technique [3] satisfies these requirements. In addition, two features are added to speed-up the analysis: First, a mixer-like analysis (with the perturbation probe being the RF input) is used to obtain the frequency response, instead of the conventional HB two-tone analysis. Second, once the frequency of the instability has been determined, the frequency sweep is restrained around that particular frequency. This allows an accurate analysis around the critical frequency with a low computing cost.

III. Application to the Design of a MMIC Power Amplifier in Ku Band

The approach is illustrated by its application to a Ku Band power amplifier for space applications. The circuit is built in coplanar monolithic technology based on HBT devices. Design goals were 2W output power with more than 20dB gain and good power-added efficiency. The integration technology is the HB20P UMS process, which uses InGaP/GaAs 2μm HBTs [5]. A power combining technique, as showed in Fig. 1, has been utilized in order to achieve such requirements.

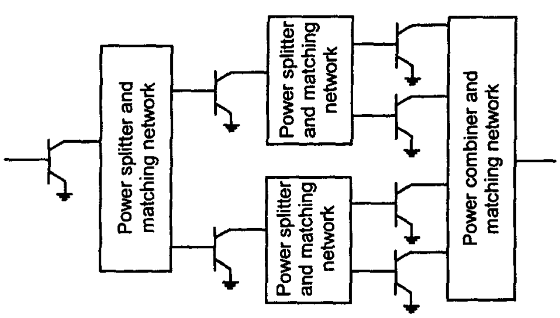

Fig. 1. Schematic of the three stage power amplifier.

A first version of this amplifier that was unstable is analyzed in section *A*. From the knowledge extracted by this analysis, a stable second version of the amplifier is re-designed in section *B*.

A. Analysis of the First Version of the Power Amplifier

Frequency division instability was experimentally found, in the first version of the amplifier, for several ranges of input power P_{in} and input frequency f_{in}. Fig. 2 shows the measured output power versus input frequency for different input power values. Only stable points are traced. The curve sections that are not represented in the figure correspond to the conditions for which the circuit was unstable.

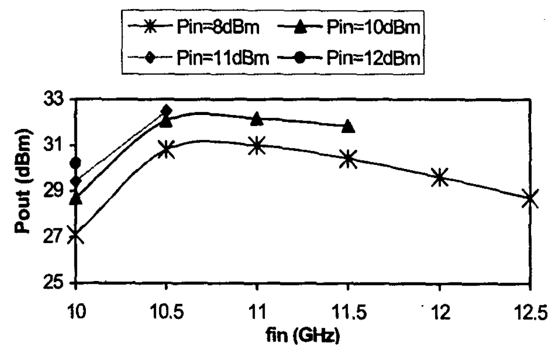

Fig. 2. First version of the amplifier. Measured output power versus input frequency for different input power values. Only stable regions are traced.

The application of the large-signal stability analysis technique to this amplifier revealed the presence of this parametric instability. Complex conjugate poles with positive real part at $f_{in}/2$ have been obtained for some values of P_{in} and f_{in}. As an example, the pole-zero map obtained for f_{in} = 11.5 GHz and P_{in}= 12 dBm is shown in Fig. 3. A couple of complex conjugate poles with positive real part at $f_{in}/2$ can be observed.

Results shown in Fig. 3 were obtained by introducing the current perturbation at a node of the amplifier second stage. The same poles are obtained when connecting the perturbation at any other node of the second stage. However, as mentioned in section II, due to the isolation provided by the matching networks, the analysis at different stages could provide different poles. Actually, complex conjugate poles with a positive real part at $f_{in}/2$ have also been detected in the third stage, but never in the first stage. This allows to locate the origin of the instability, which constitutes a useful information to modify the design.

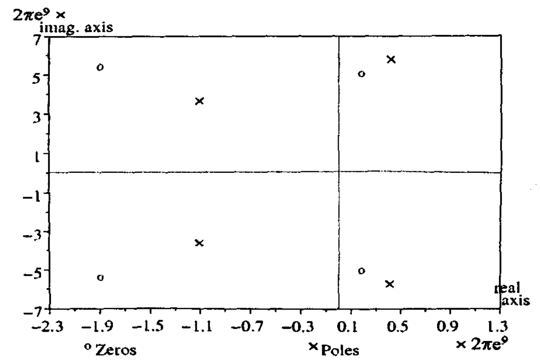

Fig. 3. Pole-zero map obtained in the second stage of the amplifier for f_{in} = 11.5 GHz and P_{in} = 12 dBm

In order to study the stability of the circuit as a function of P_{in} and f_{in}, a parametric stability analysis has been performed. The evolution of the $f_{in}/2$ poles (analyzed in the second stage) with the input frequency for P_{in} = 12 dBm is shown in Fig. 4. Observe that the $f_{in}/2$ poles become unstable as input frequency increases, which qualitatively agrees with the experimental results of Fig. 2. The quantitative discrepancies may be due to inaccuracies in the model description of the circuit elements.

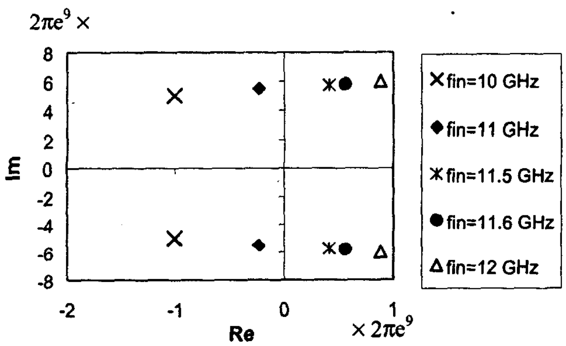

Fig. 4. The evolution of the $f_{in}/2$ poles (analyzed in the second stage) with the input frequency for P_{in} = 12 dBm

The evolution of the real part of the $f_{in}/2$ poles versus input power for f_{in} = 11.5 GHz, obtained in both second and third stages, is shown in Fig. 5. Observe that in the second stage of the amplifier, frequency division instability is detected for P_{in} higher than 5 dBm. This agrees with the trend observed experimentally. On the contrary, in the third stage, a pair of complex conjugate poles with positive real part at $f_{in}/2$ has been detected for any P_{in} value. This may imply that, even for low P_{in}, a latent instability is present, giving rise to a small steady-state $f_{in}/2$ component (under the noise level) that cannot be detected experimentally.

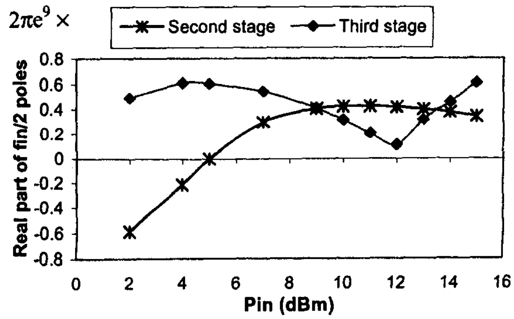

Fig. 5. Evolution of the real part of the $f_{in}/2$ poles versus input power for f_{in} = 11.5 GHz, obtained in both second and third stages

B. Elimination of the Parametric Oscillations in the Power Amplifier

A new version of the amplifier has been designed by integrating the stability analysis method in the design process. Thanks to the information on relative stability, the redesign can be focused on the operating conditions (high P_{in} and high f_{in}), where unstable poles have the larger real part. Since frequency division instabilities had been detected in the second and third stages, stabilization circuits have been introduced at the input of all the transistors in the second and third stages in order to prevent potential instabilities. Their objective is to decrease the gain at $f_{in}/2$ without modifying excessively the performances of the circuit at f_{in}.

Initially, ideal stabilization circuits have been introduced in order to verify whether circuit stabilization can be achieved by increasing the resistance at the input of the transistors. An ideal stabilization circuit can be implemented as shown in Fig. 6a. This circuit introduces a resistance R_a at $f_{in}/2$ without changing the performances of the circuit at other frequencies (Fig. 6b). Once these stabilization circuits have been included in the amplifier, a new parametric stability analysis is performed. The evolution of the real part of the poles at $f_{in}/2$ for f_{in} = 13 GHz and P_{in} = 14.23 dBm has been traced in Fig. 6c as a function of R_a. For a resistance R_a larger than 5.2 ohm the real part of the poles is negative and the circuit is stable. The analysis of the amplifier introducing ideal stabilization circuits determines, in this way, the approximate resistance value required at the divided frequency to stabilize the amplifier.

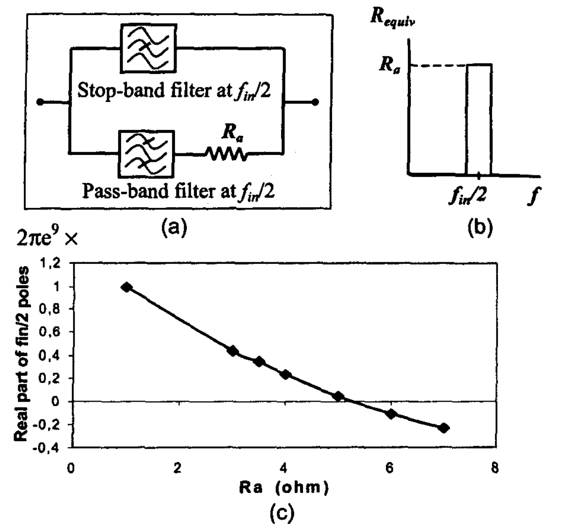

Fig. 6. (a) Ideal stabilization circuit. (b) Equivalent resistance. (c) Evolution of the real part of the poles at $f_{in}/2$ versus R_a for f_{in} = 13 GHz and P_{in} = 14.23 dBm

A high order filter should be used in practice to implement the stabilization circuit. However, for simplicity purposes and in order to minimize the chip size, a first order RC parallel filter has been used as stabilization circuit. This circuit has been introduced in series at the input of the transistors in second and third stages. The values of the RC circuit are determined by imposing the following constraints:

- The stabilization circuit should affect minimally the circuit performances at f_{in}.
- The critical poles at $f_{in}/2$ must lay on the left-half plane for any P_{in}, f_{in}.
- A sufficient stability margin considering the technological dispersion of the circuit parameters has to be guaranteed. For that, the relative position of the poles at $f_{in}/2$ has been studied by varying several critical parameters of the circuit.

Finally, a RC circuit with an equivalent resistance of 4 ohm at $f_{in}/2$ (with f_{in} = 13 GHz) stabilizes the amplifier with almost no deterioration of the circuit performances at f_{in}.

The second version of the amplifier has been fabricated and measured. The circuit is stable for any P_{in} and f_{in}. As an example, the measured output power and power added efficiency versus input power are traced in Fig. 7 for f_{in} = 11.5 GHz. Superimposed in fig 7 are the results obtained from the first version of the amplifier, up to the instability limit. As it can be observed, performances of the second version are not significantly degraded with respect to the original requirements.

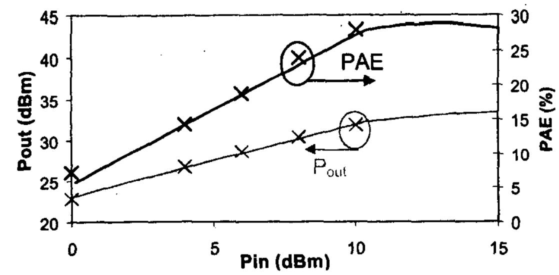

Fig. 7. Measured output power and power added efficiency versus input power for f_{in} = 11.5 GHz. Solid line: second version. Crosses: first version

IV. Conclusion

A specific approach to eliminate the risk of parametric oscillations in multistage power amplifiers has been presented. It is based on a large-signal stability technique, agile enough to be incorporated into the design process. The parametric oscillations of a Ku-band amplifier have been analyzed and eliminated through the design of a second version of the circuit by introducing specific stabilization circuitry.

Acknowledgement

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